IN THE CLAIMS

Please amend the claims as shown below. Please cancel Claim 3 without prejudice. This listing of claims will replace all prior versions and listings of claims in the Application.

1. (Currently Amended) In a microcontroller with an embedded processor, a switched mode pump power supply and power on reset circuit, ~~said processor and said power on reset circuit interconnectedly coupled, and said power supply interconnectedly coupled with said power on reset circuit and responsive to signals therefrom,~~ a method of dynamically controlling a plurality of power stability functions for said microcontroller, said method comprising ~~the steps of~~:

a) supplying a power state to said microcontroller from said switched mode pump power supply, wherein said processor and said power on reset circuit are interconnectedly coupled, and wherein said switched mode pump power supply is interconnectedly coupled with said power on reset circuit and responsive to signals therefrom;

b) sensing a power state condition of said power state;

c) determining a suitability status of said power state condition;

d) communicating said suitability status between said power on reset circuit and said processor;

e) controlling certain functions of said microcontroller accordingly.

2. (Currently Amended) The method as recited in Claim 1, further comprising ~~the step of~~:

f) dynamically programming said power on reset circuit.

3. (Cancelled)

4. (Original) The method as recited in Claim 2, wherein said power on reset circuit and said processor are interconnected via a bus.

5. (Currently Amended) The method as recited in Claim 4, wherein said ~~step~~ b) and said ~~step~~ c) are accomplished by said power on reset circuit.

6. (Currently Amended) The method as recited in Claim 5, wherein said ~~step~~ b) further comprises sensing a common supply voltage, wherein said common supply voltage is the voltage of said power state.

7. (Currently Amended) The method as recited in Claim 6, wherein said ~~step~~ c) further comprises:

c1 ~~b1~~) generating a precision reference voltage;

c2 ~~b2~~) dividing said common supply voltage into a plurality of aspect voltages, each of said plurality of aspect voltages corresponding to separate voltage quantity, each separate voltage quantity an independent multiple of said common supply voltage;

c3 ~~b3~~) forming a plurality of comparisons, each of said plurality of comparisons comparing one of said plurality of aspect voltages to said precision reference voltage; and

c4 ~~b4~~) generating a plurality of power state condition signals, each of said plurality of power state condition signals corresponding to one of each of said plurality of comparisons.

8. (Original) The method as recited in Claim 7, wherein said precision reference voltage is independent of said common supply voltage.

9. (Original) The method as recited in Claim 8, wherein said independent multiple of said common supply voltage is, selectively, fixed and programmable.

10. (Currently Amended) The method as recited in Claim 9, wherein said ~~step~~ b2) is performed by a power supply scaler, and wherein said power supply scaler comprises:

a) a divider of said common supply voltage;

b) a matrix of multiplexers and registers, and

c) an interconnection to said bus.

11. (Currently Amended) The method as recited in Claim 10, wherein said ~~step~~ d) and ~~step~~ f) are conducted via said bus.

12. (Currently Amended) The method as recited in Claim 11, wherein said ~~step~~ f) is performed by said microprocessor, and further comprises ~~the steps of~~:

f1) ascertaining a status of said microcontroller;

f2) determining an optimal power state corresponding to said status;

f3) programmatically calculating an optimal value for each programmable said independent multiple of said common supply voltage;

f4) setting each said optimal value; and

f5) repeating said ~~steps~~ f1) through f4).

13. (Currently Amended) The method as recited in Claim 12, wherein said ~~step~~ f4) further comprises:

communicating each said optimal value to said power supply scaler via said bus;

registering each said optimal value with said matrix of multiplexers and registers;

commanding said matrix of multiplexers and registers to change said independent multiple of said common supply voltage to correspond with said optimal value; and

monitoring said matrix of multiplexers and registers.

14. (Currently Amended) In a microcontroller, a system~~, said system~~ comprising:

~~a power supply;~~

a bus;

a processor coupled to said bus;~~ and a power on reset circuit, said processor and said power on reset circuit coupled to said bus and interconnectedly coupled with said processor via said bus; and~~

a power on reset circuit, said processor and said power on reset circuit coupled to said bus and interconnectedly coupled with said processor via said bus; and

a switched mode pump power supply interconnectedly coupled with said power on reset circuit and responsive to signals therefrom~~;~~

~~said system executing~~ wherein said system executes a method of dynamically controlling a plurality of power stability functions for said microcontroller, said method comprising~~: the steps of:~~

a) supplying a power state to said microcontroller from said switched mode pump power supply;

b) sensing a power state condition of said power state;

c) determining a suitability status of said power state condition;

d) communicating said suitability status between said power on reset circuit and said processor via said bus;

e) controlling certain functions of said microcontroller according to said suitability status ~~accordingly~~; and

f) dynamically programming said power on reset circuit via said bus.

15. (Currently Amended) The system as recited in Claim 14, wherein said ~~step~~ b) and said ~~step~~ c) of said method are accomplished by said power on reset circuit.

16. (Currently Amended) The system as recited in Claim 15, wherein said ~~step~~ b) of said method further comprises sensing a common supply voltage, wherein said common supply voltage is the voltage of said power state.

17. (Currently Amended) The system as recited in Claim 16, wherein said ~~step~~ c) ~~of said method~~ further comprises:

c1 ~~b1~~) generating a precision reference voltage, said precision reference voltage independent of said common supply voltage;

c2 ~~b2~~) dividing said common supply voltage into a plurality of aspect voltages, each of said plurality of aspect voltages corresponding to separate voltage quantity, each separate voltage quantity an independent multiple of said common supply voltage;

c3 ~~b3~~) forming a plurality of comparisons, each of said plurality of comparisons comparing one of said plurality of aspect voltages to said precision reference voltage; and

c4 ~~b4~~) generating a plurality of power state condition signals, each of said plurality of power state condition signals corresponding to one of each of said plurality of comparisons.

18. (Currently Amended) The system as recited in Claim 17, wherein said ~~step~~ b2) ~~of said method~~ is performed by a power supply scaler, wherein said power supply scaler comprises:

a) a divider of said common supply voltage;

b) a matrix of multiplexers and registers, and

c) an interconnection to said bus.

19. (Currently Amended) The system as recited in Claim 18, wherein said ~~step~~ f) ~~of said method~~ is performed by said microprocessor, and further comprises: ~~the steps of:~~

f1) ascertaining a status of said microcontroller;

f2) determining an optimal power state corresponding to said status;

f3) programmatically calculating an optimal value for each programmable said independent multiple of said common supply voltage;

f4) setting each said optimal value; and

f5) repeating said ~~steps~~ f1) through f4).

20. (Currently Amended) The method as recited in Claim 19, wherein said ~~step~~ f4) further comprises:

communicating each said optimal value to said power supply scaler via said bus;

registering each said optimal value with said matrix of multiplexers and registers;

commanding said matrix of multiplexers and registers to change said independent multiple of said common supply voltage to correspond with said optimal value; and

monitoring said matrix of multiplexers and registers.

21. (Currently Amended) In a microcontroller having a power on reset circuit interconnected with a processor~~, said microcontroller having a power state powered by a power supply, said power supply interconnected with and responsive to control by said power on reset circuit,~~ a method of dynamically controlling said power state, said method comprising ~~the steps of~~:

a) ascertaining a ~~said~~ power state powered by a switched mode pump power supply, said switched mode pump power supply interconnected with and responsive to control by said power on reset circuit;

b) programmatically determining desired changes to said power state;

c) intercommunicating between said processor and said power on reset circuit;

d) adjusting said power on reset circuit corresponding to said desired changes to said power state;

e) controlling said switched mode pump power supply according to said d)~~; correspondingly;~~ and

f) repeating said ~~steps~~ a) through e).